REMARKS

Claims 1-23 will be pending upon entry of the present amendment. Claims 12 and 15 have been amended. Claim 23 is new. No new matter has been added by way of this amendment.

Claims 1-3 were rejected under 35 U.S.C. § 102(e) as being anticipated by Walters et al., U.S. Patent No. 6,453,281 ("Walters").

An embodiment of the present invention provides an electronic device for the recording/reproduction of voice data that is entirely integrated in a chip of semiconductor material. It should be emphasized that the components of the electronic device, including the main transmission line, control unit, signal-conversion unit and non-volatile memory unit, are *all integrated in the same chip*. The advantages of this single-chip integration include a smaller device size and reduced power consumption. In addition, the unique architecture of the single-chip integration enables the device to optimize editing of the voice messages itself. Furthermore, the embodiment is characterized by the ability to accept and emit audio signals according to different formats by virtue of an interface circuit. This interface circuit adapts the format of data exchanged between the signal-conversion unit and the memory unit and implements a strategy of recovery of commands lost or failed.

Claim 1 recites "An electronic device for the recording/reproduction of voice data, comprising: a chip of semiconductor material; a main transmission line *integrated in said chip*; a control unit *integrated in said chip*...; a signal-conversion unit *integrated in said chip*...; and a non-volatile memory unit *integrated in said chip*..." (Emphasis added.) There is nothing disclosed in Walters with regard to an electronic device for the recording/reproduction of voice data wherein the components of the electronic device (including the main transmission line, control unit, signal-conversion unit and non-volatile memory unit) are all integrated in the same chip. In contrast, Walters discloses an audio database device that is comprised of separate discrete components or integrated circuits mounted on a board (Figures 5-7B and the corresponding description). This is the exact *opposite* of the unique single-chip integration of the present invention.

Therefore, because Walters does not disclose all of the recited elements of claim 1, claim 1 is not anticipated by Walters and is in condition for allowance. Claims 2 and 3 depend on claim 1, and thus, are also in condition for allowance.

Claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters in view of Unno et al., EP 0 851 423 A1 ("Unno").

Walters and Unno do not teach or suggest the invention recited in claims 4 and 5. Unno does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Walters do not include all of the recited elements of claim 1, modifying the teachings of Walters by incorporating the teachings of Unno (a buffer memory) would not satisfy the limitations of claims 4 and 5.

Because Walters and Unno together do not disclose, teach or suggest all of the recited elements of claims 4 and 5, claims 4 and 5 are not unpatentable over Walters in view of Unno and are in condition for allowance.

Claims 6 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters in view of Unno and further in view of Daberko, U.S. Patent No. 5,787,445 ("Daberko").

Walters, Unno and Daberko do not teach or suggest the invention recited in claims 6 and 7. Daberko does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Walters do not include all of the recited elements of claim 1, modifying the teachings of Walters by incorporating the teachings of Unno (a buffer memory) and Daberko (first and second cache memories) would not satisfy the limitations of claims 6 and 7.

Because Walters, Unno and Daberko together do not disclose, teach or suggest all of the recited elements of claims 6 and 7, claims 6 and 7 are not unpatentable over Walters in view of Unno and further in view of Daberko and are in condition for allowance.

Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters in view of Unno and further in view of Rossum, U.S. Patent No. 6,016,522 ("Rossum").

Walters, Unno and Rossum do not teach or suggest the invention recited in claim 8. Rossum does not disclose anything about a single-chip integrated electronic device as recited

in claim 1. Therefore, because the teachings of Walters do not include all of the recited elements of claim 1, modifying the teachings of Walters by incorporating the teachings of Unno (a buffer memory) and Rossum ("ping-pong" buffering) would not satisfy the limitations of claim 8.

Because Walters, Unno and Rossum together do not disclose, teach or suggest all of the recited elements of claim 8, claim 8 is not unpatentable over Walters in view of Unno and further in view of Rossum and is in condition for allowance.

Claims 9-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters in view of Ogawa, U.S. Patent No. 6,604,168 ("Ogawa").

Walters and Ogawa do not teach or suggest the invention recited in claims 9-11. Ogawa does not disclose anything about a single-chip integrated electronic device as recited in claim 1. In addition, Ogawa simply discloses a flash ROM (15) having a memory area (151), where each memory area (151) stores both the data (157) and the corresponding management information (152-156). As a result, the data and the management information are stored in the same single memory area (151) (Figure 4; column 14, lines 48-59; column 15, lines 2-4). This is completely different from the present invention that uses a first memory area (28) for storing the data, and a second memory area (29) for storing the corresponding management information. This makes it possible to erase the data (in the first memory area) without erasing the corresponding management information (in the second memory area). Therefore, because the teachings of Walters do not include all of the recited elements of claim 1, modifying the teachings of Walters by incorporating the teachings of Ogawa (a single memory area) would not satisfy the limitations of claims 9-11.

Because Walters and Ogawa together do not disclose, teach or suggest all of the recited elements of claims 9-11, claims 9-11 are not unpatentable over Walters in view of Ogawa and are in condition for allowance.

Claims 12, 13, 15 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters in view of Unno.

Claims 12 and 15 have been amended to clarify that the components are integrated in the same chip. As discussed above, Unno does not disclose anything about an integrated method or electronic device as recited in claims 12 and 15. Therefore, because the

teachings of Walters do not include all of the recited elements of claim 12 and 15, modifying the teachings of Walters by incorporating the teachings of Unno (a buffer memory) would not satisfy the limitations of claims 12 and 15.

Because Walters and Unno together do not disclose, teach or suggest all of the recited elements of claims 12 and 15, claims 12 and 15 are not unpatentable over Walters in view of Unno and are in condition for allowance. Claim 13 depends on claim 12 and claim 16 depends on claim 15, and thus, are also in condition for allowance.

Claims 14 and 17-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters in view of Unno and further in view of Rossum.

As discussed above, Rossum does not disclose anything about an integrated method or electronic device as recited in claims 12 and 15. Therefore, because the teachings of Walters do not include all of the recited elements of claims 12 and 15, modifying the teachings of Walters by incorporating the teachings of Unno (a buffer memory) and Rossum ("ping-pong" buffering) would not satisfy the limitations of claims 14 and 17-19.

Because Walters, Unno and Rossum together do not disclose, teach or suggest all of the recited elements of claims 14 and 17-19, claims 14 and 17-19 are not unpatentable over Walters in view of Unno and further in view of Rossum and are in condition for allowance.

Claims 20-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters in view of Unno and further in view of Ogawa.

As discussed above, Ogawa does not disclose anything about an integrated method or electronic device as recited in claims 12 and 15. Therefore, because the teachings of Walters do not include all of the recited elements of claims 12 and 15, modifying the teachings of Walters by incorporating the teachings of Unno (a buffer memory) and Ogawa (a single memory area) would not satisfy the limitations of claims 20-22.

Because Walters, Unno and Ogawa together do not disclose, teach or suggest all of the recited elements of claims 20-22, claims 20-22 are not unpatentable over Walters in view of Unno and further in view of Ogawa and are in condition for allowance.

New claim 23 depends on claim 1, and thus, is allowable for the reasons expressed above. In addition, claim 23 recites that the non-volatile memory unit includes a

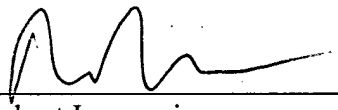
format adapter for adapting the format of the first stream of compressed digital signal for the non-volatile memory unit (see page 4, line 27 though page 5, line 2 for support). None of the cited prior art teaches or suggests such a format adapter. Thus, claim 23 is in condition for allowance.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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